**Lab 01 – SRAM Stability Analysis**

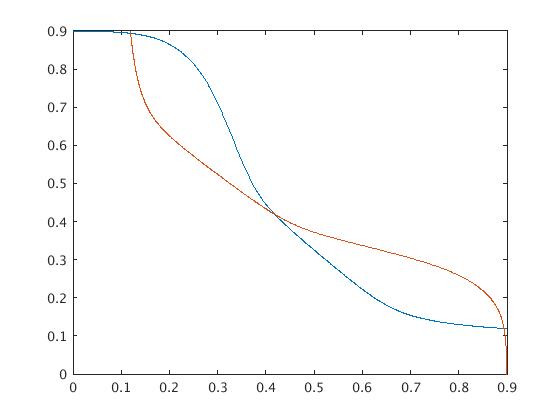
**Design:**

6T SRAM cell is built with the cell ratio of **2:1:1 (PD: PG: PU)** having a stronger PD compared to PU and PG with minimum width of **35nm** and minimum gate length of **30nm** and VDD of **0.9V.** In this lab, we will be observing the static and dynamic stability of SRAM cell operation and its dependencies.

**Part 1: Static Stability Analysis**

1. **Butterfly curve – Read mode of SRAM cell**

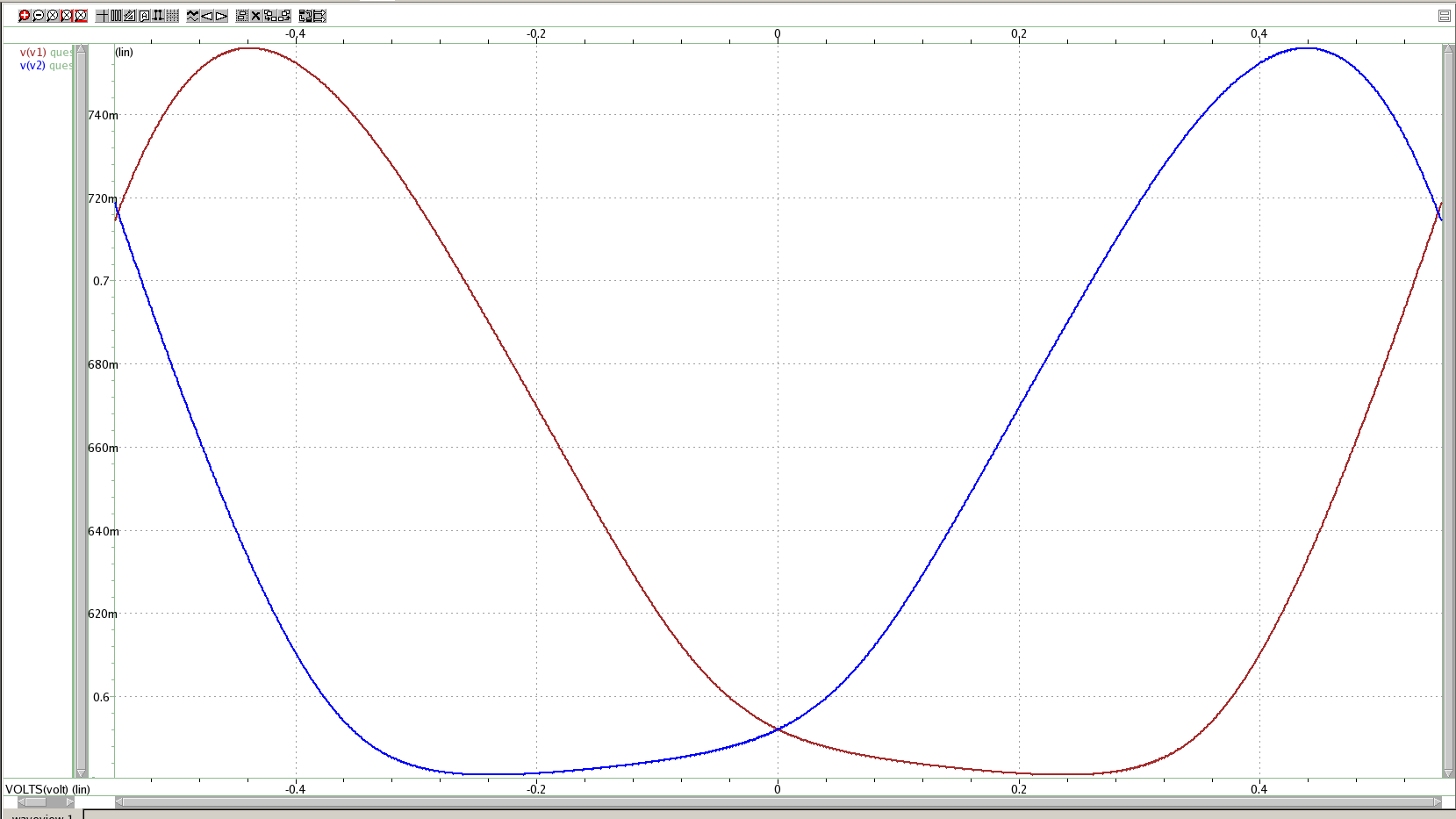
We consider only one half circuit with just on PG, PD and PU with BL and BLB pre-charged to VDD and WL to VDD. By varying the input signal, we could sweep input voltage and observe output. For the butterfly curve, we just invert the axes and the butterfly curve for SRAM operated in Read mode is obtained.

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*Fig1: Butterfly curve in read operation*

1. **Read Margin Calculation**
   1. **SNM for SRAM Read**

We develop the whole SRAM cell and obtain the butterfly curve. By reading the paper, we determine the SNM by rotating the butterfly curve by an angle of 45 degrees and determine the diagonal of the largest square that can be fit inside the curve.



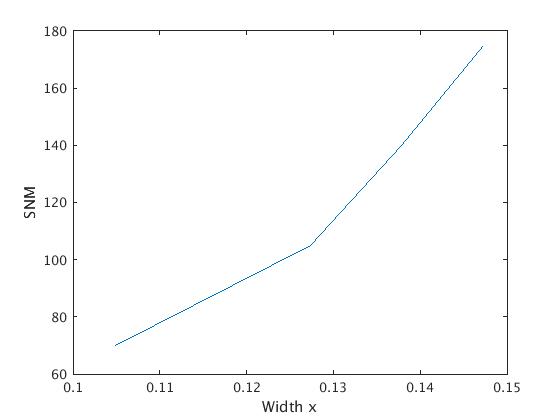
*Fig 2: 45 degree rotated butterfly curve for SNM calculation*

SNM for SRAM read = **0.1049**

* 1. **SNM dependency on Width of PD NMOS**

The width of PD NMOS is varied from 70nm to 175nm in steps of 35nm and determine SNM for each width. We observe that as we increase the width of PD NMOS, Static Noise margin in read mode increases.

As we increase the width of PD-NMOS, the butterfly curve gets shifted left, resulting in a higher SNM. In other words, when we apply a noise at the node Q, the node voltage at Q tends to increase. By having a stronger PD-NMOS, helps in maintaining the node voltage at Q at 0. Hence having a good Static noise margin.

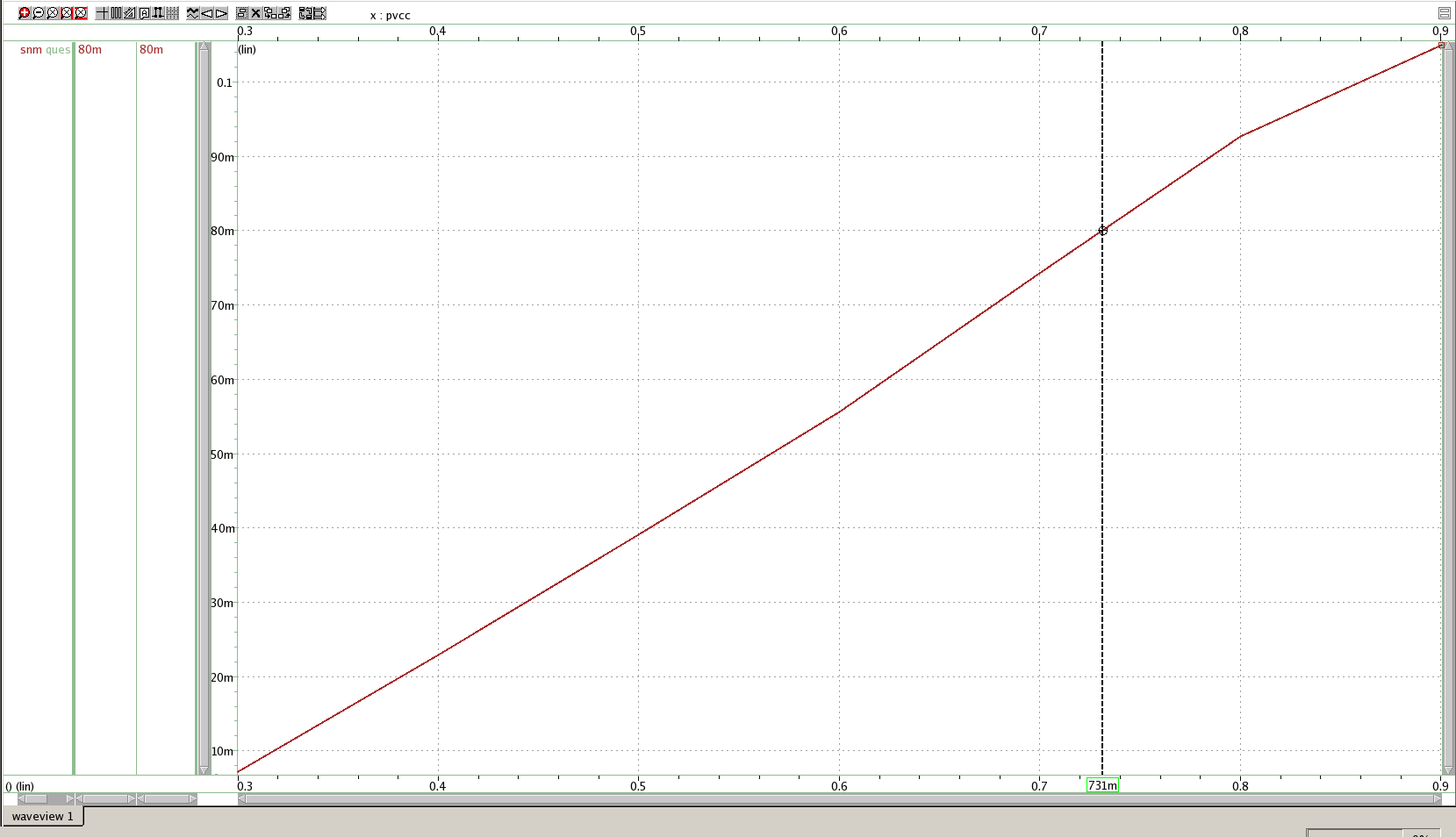


*Fig 3: SNM dependency on Width of PD-NMOS*

* 1. **SNM dependency on VDD**

The voltage at VDD is varied from 0.3V to 0.9V in steps of 0.1V and determine SNM at each VDD. We observe that as we increase the VDD, Static Noise margin in read mode increases.

VDD plays a key role in determining the swing of output at Q and the size of square in the butterfly curve. As we decrease VDD, the butterfly curve falls short, reducing the net area available for the square, thus a poor SNM at lower VDD.



*Fig 4: SNM dependency on VDD*

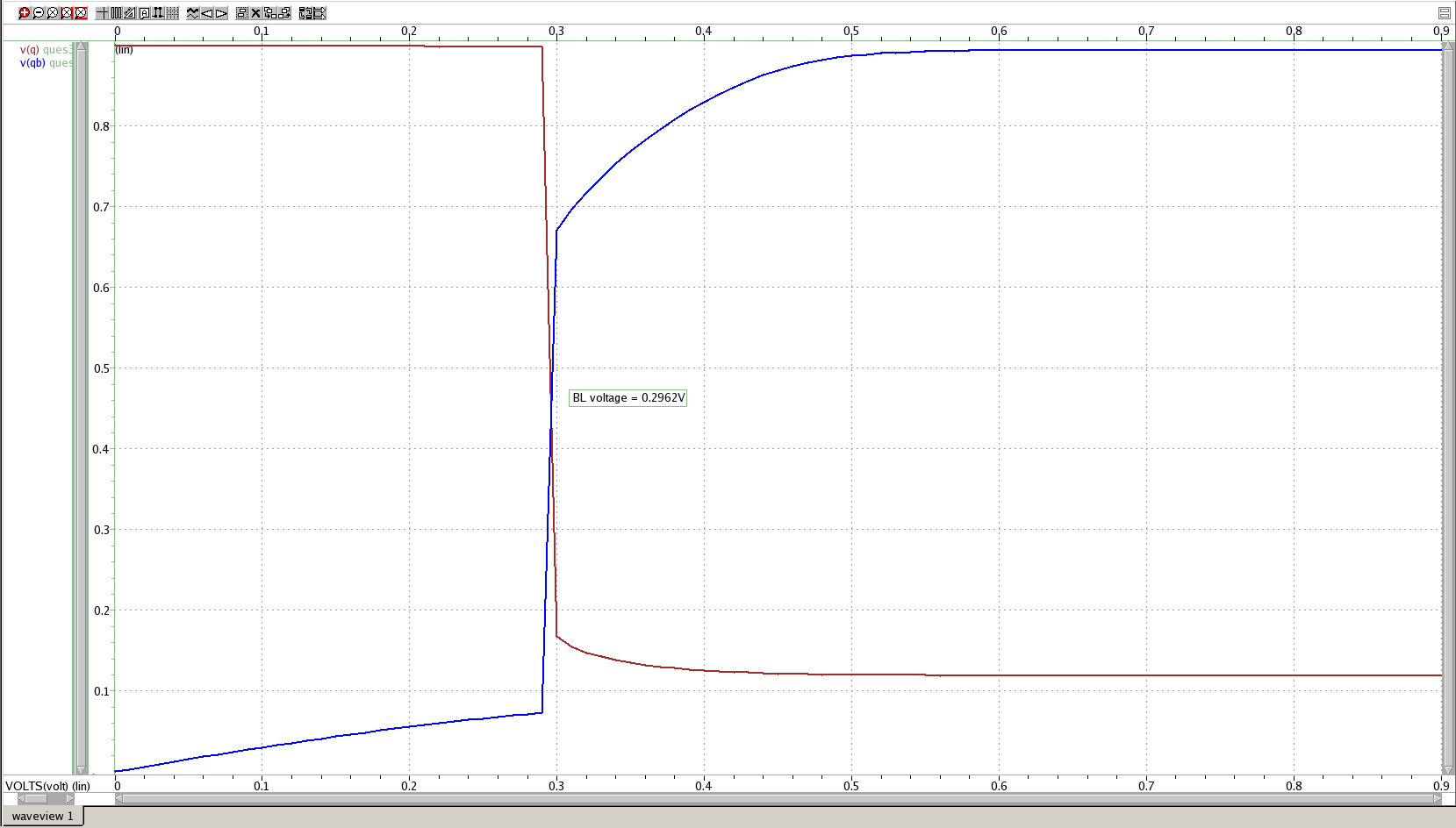
For the system to be stable, SNM should be minimum at 80 mV, hence the optimum VDD for a stable operation is found to be **0.731V**.

1. **Static Write Margin Calculation**
   1. **SNM calculation in Write mode**

To operate the SRAM in write mode, we pre-charge BL to VDD and BLB to GND and WL to VDD. The whole SRAM circuit is developed to operate SRAM cell in write mode. The node voltages of Q and Qb are set at VDD and GND initially.

In order to calculate Write SNM, we utilize the method mentioned in the paper. WSNM is the BL voltage at which Q and QB flips.

WSNM = **0.2962V**

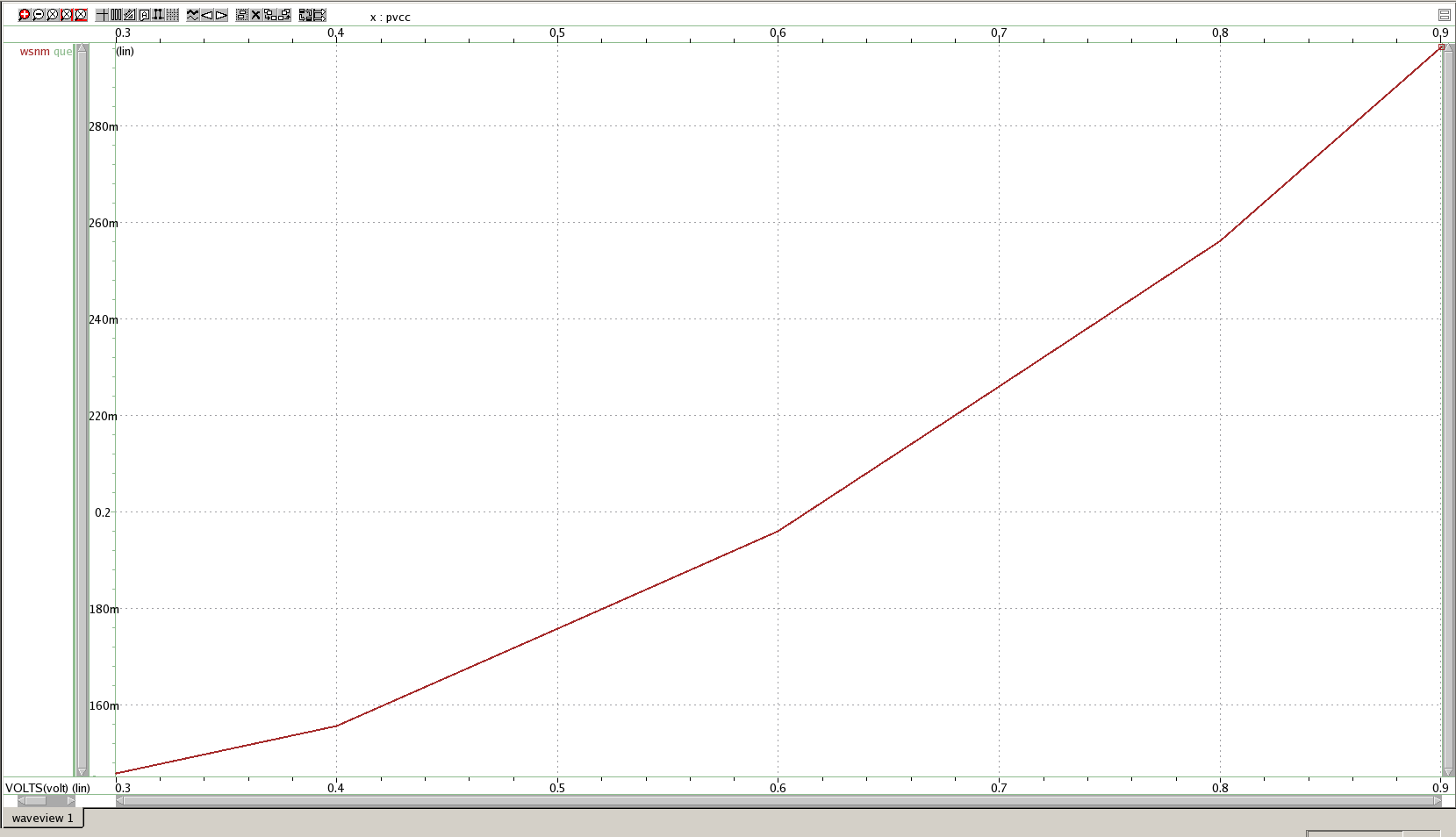


*Fig 5: Write margin Calculation*

* 1. **WSNM dependency on VDD**

The voltage at VDD is varied from 0.3V to 0.9V in steps of 0.1V and determine SNM at each VDD. We observe that as we increase the VDD, Static Noise margin in write mode increases.

VDD plays a key role in determining the limits of logic 0 and logic 1. As we decrease VDD, the node voltages become more susceptible to noise. Since SNM is the measure of susceptibility of SRAM cell to noise, SNM decreases as we decrease VDD.

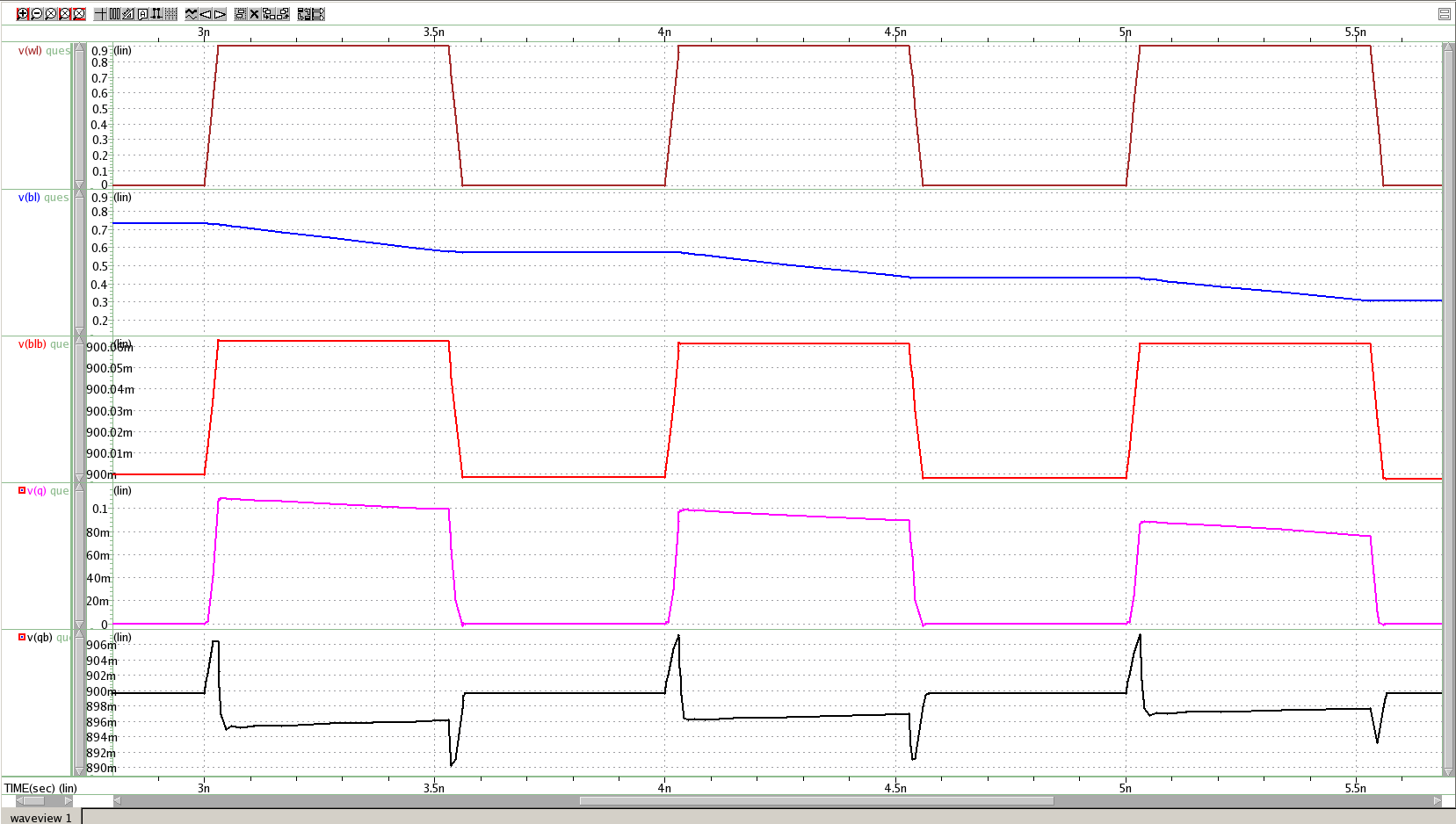
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*Fig 6: WSNM dependency on VDD*

**Part 2: Dynamic Stability Analysis**

1. **Dynamic Read**

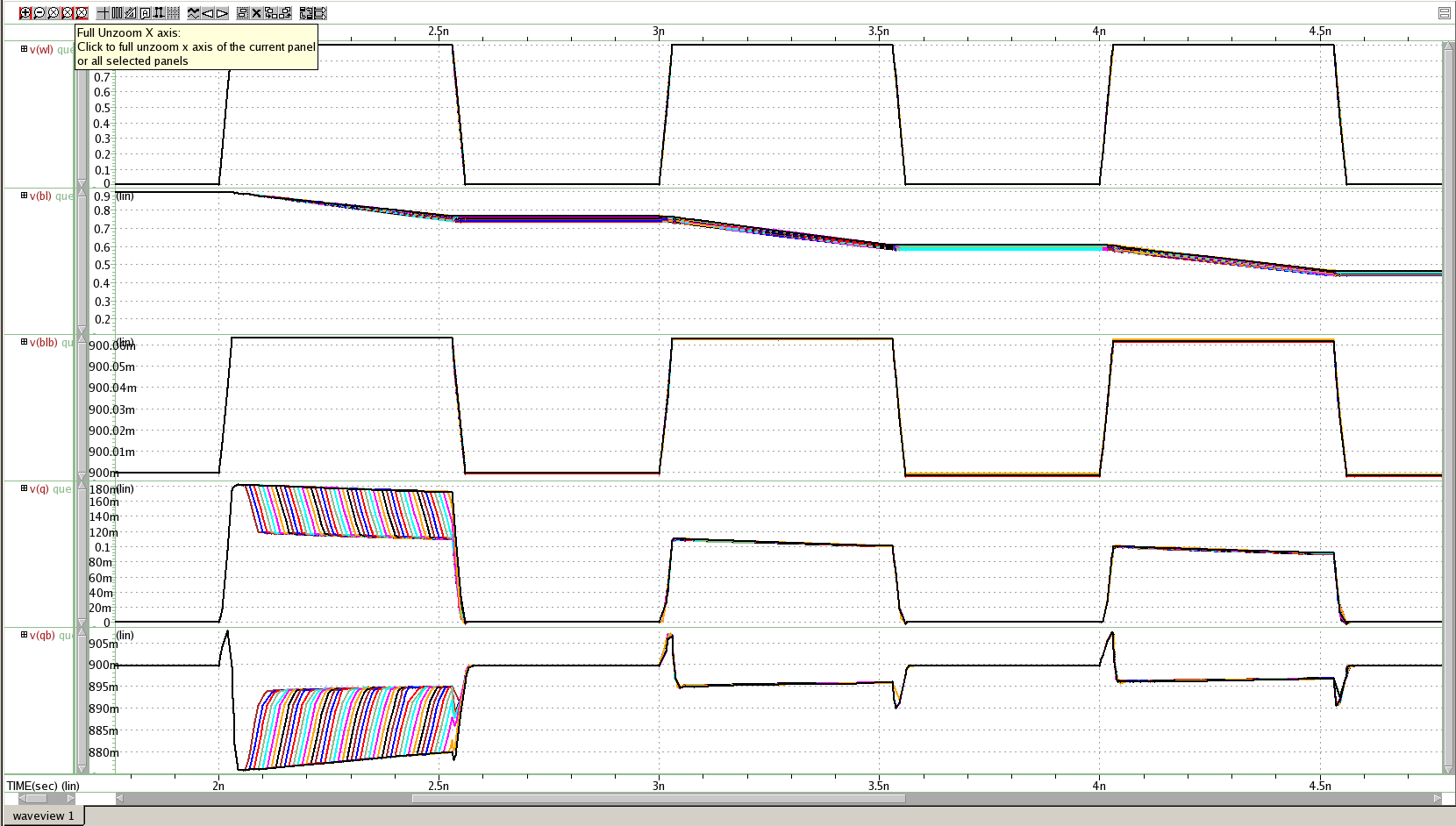
The read operation is performed by pre-chargingBL and BLB to VDD and sweeping WL in a transient manner. The node voltages at Q and Qb are set at VDD and GND.



*Fig 7: Dynamic read operation*

1. **Noise dependency on SNM**

A noise current of 20mA is introduced at node Q and the node voltages at Q and QB are observed with respect to WL, BL and BLB to determine the noise dependency of SNM in dynamic read operation. On observing the waveforms we could realize that even after adding a noise current of 20 mA, the read operation doesn’t fail.

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*Fig 8: Dynamic read operation with noise current 20 mA*

1. **Noise Dependency – Read failure**

A noise current of 35mA is introduced at node Q and the node voltages at Q and QB are observed with respect to WL, BL and BLB to determine the noise dependency of SNM in dynamic read operation. On observing the waveforms we could realize that after adding a noise current of 35 mA, the read operation fails, since Q and Qb flips resulting in an unintended write.

Critical charge is the minimal amount of charge injected by noise leads to a READ failure. In our case, Read failure happens at 80ps pulse width of noise. Hence critical charge is determined as follows.

Critical charge = Current \* Pulse width

= 35uA \* 80ps

= 2800e-18

= 2.8fC



*Fig 9: Read failure due to noise current of 35 mA*

**APPENDIX**

**Part 1: Static Stability Analysis**

**Q2 Part 3:** Read Noise Margin Vs VDD

**Ques2c sp file**

\* SNM for Read SRAM

.GLOBAL vcc!

+ gnd!

.SUBCKT sram1 wl bl in out

\*Pass Gate

MM0 bl wl out gnd! nmos w=35n l=30n

\*Pull Down

MM1 out in gnd! gnd! nmos w=70n l=30n

\*Pull Up

MM2 out in vcc! vcc! pmos w=35n l=30n

.ENDS

**Ques2c tb file**

\* Part 1 - Static Stability Analysis

\* Question 2 - partc - Read Margin Vs VDD

.TEMP 25

.OPTION

.include "/afs/asu.edu/users/a/p/a/aparame2/Memories/32nm\_HP.pm"

.include "./ques2c.sp"

\* Variable u and pvcc can be swept

.param u=0

.param pvcc=0V

Vgnd gnd! 0 DC=0V

Vvdd vcc! 0 DC=pvcc

\* SRAM full circuit in Read Mode

X\_hf1 wl1 bl1 in1 out1 sram1

X\_hf2 wl2 bl2 in2 out2 sram1

Vwl1 wl1 0 DC=pvcc

Vbl1 bl1 0 DC=pvcc

Cbl1 bl1 0 100f

Vwl2 wl2 0 DC=pvcc

Vbl2 bl2 0 DC=pvcc

Cbl2 bl2 0 100f

\*in1 and in2 are already defined as VCVS no need for voltage sources

Evx v1 0 VOL='(sqrt(2)\*V(out1))+u'

Ex in1 0 VOL='((1/sqrt(2))\*u)+((1/sqrt(2))\*V(v1))'

Evy v2 0 VOL='(sqrt(2)\*V(out2))-u'

Ey in2 0 VOL='(((1/sqrt(2))\*V(v2))-(1/sqrt(2))\*u)'

Exy v12 0 VOL='V(v1)-V(v2)'

\* SNM Calculation

.measure DC maxi MAX V(v12)

.measure DC mini MIN V(v12)

.measure DC absmin PARAM='sqrt(mini\*mini)'

.measure DC absmax PARAM='sqrt(maxi\*maxi)'

.measure DC minx PARAM='MIN(absmin,absmax)'

.measure DC snm param='minx/1.414'

.DC u '-(pvcc/1.414)' 'pvcc/1.414' 0.001 pvcc 0.9 0.3 -0.1

.probe v(\*)

.option post

.end

**Q3 Part 2:** Write Noise Margin Vs VDD

**Ques3b sp file**

\* Write margin

.GLOBAL vcc!

+ gnd!

.SUBCKT sram1 wl bl in out

\*PG1

MM0 bl wl out gnd! nmos w=35n l=30n

\*PD1

MM1 out in gnd! gnd! nmos w=70n l=30n

\*PU1

MM2 out in vcc! vcc! pmos w=35n l=30n

.ENDS

**Ques3b tb file**

\* Part 1 - Static Stability Analysis

\* Ques 3a - Write Margin Vs VDD

.TEMP 25

.OPTION MEASFORM=3

.param pvcc=0.9V

.include "/afs/asu.edu/users/a/p/a/aparame2/Memories/32nm\_HP.pm"

.include "./ques3b.sp"

Vgnd gnd! 0 DC=0V

Vvdd vcc! 0 DC=pvcc

X\_hf1 wl bl qb q sram1

X\_hf2 wl blb q qb sram1

Vwl wl 0 DC=pvcc

Vblb blb 0 DC=pvcc

Vbl bl 0 DC=pvcc

\* Set node voltages q and qb to VDD and 0V

.NODESET qb pvcc q 0

.DC Vblb 0.9 0 -0.01 pvcc 0.9 0.3 -0.1

\* Calculate Write Margin when Q and Qb flips

.measure DC WSNM FIND V(blb) WHEN V(q) = V(qb)

.probe v(\*)

.option post

.end

**Part 2: Dynamic Stability Analysis**

**SNM VS Noise magnitude of 35uA**

**Ques1c sp file**

\* Dynamic Read Margin

.GLOBAL vcc!

+ gnd!

.SUBCKT sram1 wl bl in out

\*PG

MM0 bl wl out gnd! nmos w=35n l=30n

\*PD

MM1 out in gnd! gnd! nmos w=70n l=30n

\*PU

MM2 out in vcc! vcc! pmos w=35n l=30n

.ENDS

**Ques1c tb file**

\* Part2 - Dynamic Stability Analysis

\* Ques1c - Noise in Dynamic Read operation

.TEMP 25

.OPTION

.param tr=30p

.param tf=30p

.param pw=500p

.param pw1=500p

.param period=8n

.param vdd=0.9V

.include "/afs/asu.edu/users/a/p/a/aparame2/Memories/32nm\_HP.pm"

.include "./ques1c.sp"

Vgnd gnd! 0 DC=0V

Vvdd vcc! 0 DC=0.9V

X\_hf1 wl bl qb q sram1

X\_hf2 wl blb q qb sram1

\* IC is used to set node voltages in Transient mode

.IC V(qb)=0.9V V(q)=0 V(bl)=0.9V V(blb)=0.9V

Vwl wl 0 PULSE (0 0.9 2000p tr tf pw 1000p)

\*Noise Current added

In 0 q PULSE (0 35u 2000p tr tf pw1 period)

Cbl bl 0 100f

Cblb blb 0 100f

.tran 2p 8n UIC SWEEP pw1 30p 500p 10p

.probe v(\*)

.probe i(\*)

.option post

.end